UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,689	03/30/2004	Thomas J. Foster	H10415/JDP	4031

1333 7590 07/02/2007

EASTMAN KODAK COMPANY
PATENT LEGAL STAFF
343 STATE STREET
ROCHESTER, NY 14650-2201

EXAMINER	
VO, QUANG N	

ART UNIT	PAPER NUMBER
2625	

MAIL DATE	DELIVERY MODE
07/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,689	FOSTER ET AL.	
	Examiner	Art Unit	
	Quang N. Vo	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/27/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 7 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 7 of U.S. Patent No. 6,975,411. Although the conflicting claims are not identical, they are not patentably distinct from each other because the limitations of claims 1, 7 in application are similar to claim 7 in US Patent 6,975,411.

Regarding claim 1, it is drawn to a method of altering the appearance of an input digital image when printed, the digital image comprised of an array of pixels and wherein each pixel is assigned a digital value representing marking information, the method comprising the steps of: defining each pixel as either a

background pixel, interior pixel, edge pixel, one line pixel, or two line pixel; and, reassigning the digital value of one or more interior pixels, edge pixels, one line pixels, or two line pixels independently.

Regarding claim 7 of US Patent 6,975,411 it discloses an electrostatographic recording method for printing an image on a receiver comprising the steps of: operating a primary charger to establish a uniform primary voltage level on an image recording member; developing a control patch on the image recording member, measuring density of the control patch to thereby provide a density measurement signal; converting the image into a digital bitmap comprised of an array of pixels wherein each pixel is assigned a digital value representing marking information; rendering the digital bitmap by defining each pixel as either a background pixel, interior pixel, edge pixel, one line pixel, or two line pixel and reassigning the digital value of one or more interior pixels, edge pixels, one line pixels, or two line pixels independently and as a function of the density measurement signal; and, modulating electrostatic charge on the image recording member as a function of the digital bitmap after rendering.

The subject matter claimed in claim 1 is fully disclosed in claim 7 of the referenced US Patent 6,975,411 as follow: the digital image comprised of an array of pixels and wherein each pixel is assigned a digital value representing marking information, the method comprising the steps of: defining each pixel as either a background pixel, interior pixel, edge pixel, one line pixel, or two line pixel; and, reassigning the digital value of one or more interior pixels, edge pixels, one line pixels, or two line pixels independently.

Regarding claim 7, it is drawn to a method of printing an image comprising the steps of: converting the image into a digital bitmap comprised of an array of pixels wherein each pixel is assigned a digital value representing marking information; defining each pixel as a background pixel, interior pixel, edge pixel, one line pixel, or two line pixel; and, reassigning the digital value of one or more interior pixel, edge pixel, one line pixel, or two line pixels independently, thereby altering the appearance of the image when printed.

See above for claim 7 of US Patent 6,975,411.

The subject matter claimed in claim 7 is fully disclosed in claim 7 of the referenced US Patent 6,975,411 as follow: converting the image into a digital bitmap comprised of an array of pixels wherein each pixel is assigned a digital value representing marking information; defining each pixel as a background pixel, interior pixel, edge pixel, one line pixel, or two line pixel; and, reassigning the digital value of one or more interior pixel, edge pixel, one line pixel, or two line pixels independently, thereby altering the appearance of the image when printed.

Claims 14, 19 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim(s) 19 of U.S. Patent No. 6,975,411. Although the conflicting claims are not identical, they are not patentably distinct from each other because the limitations of claims 14, 19 in application are similar to claim 19 in US Patent 6,975,411.

Regarding claim 14, it is drawn to an apparatus for altering the appearance of an input digital image when printed, the digital image comprised of

an array of pixels and wherein each pixel is assigned a digital value representing marking information, the apparatus comprising: a rendering circuit for defining each pixel as either a background pixel, interior pixel, edge pixel, one line pixel, or two line pixel; and, reassigning the digital value of one or more interior pixels, edge pixels, one line pixels, or two line pixels independently.

Regarding claim 19 of US Patent 6,975,411 it discloses an electrostatographic printing apparatus for printing an image on a receiver comprising: a primary charger to establish a uniform primary voltage level on an image recording member; a developer for developing a control patch on the image recording member, a densitometer for measuring density of the control patch to thereby provide a density measurement signal; a raster image processor for converting the image into a digital bitmap comprised of an array of pixels wherein each pixel is assigned a digital value representing marking information a rendering circuit for rendering the digital bitmap by defining each pixel as either a background pixel, interior pixel, edge pixel, one line pixel, or two line pixel and reassigning the digital value of one or more of edge pixels or interior pixels independently and as a function of the density measurement signal; wherein the developer modulates electrostatic charge on the image recording member as a function of the digital bitmap after rendering.

The subject matter claimed in claim 14 is fully disclosed in claim 19 of the referenced US Patent 6,975,411 as follow: the digital image comprised of an array of pixels and wherein each pixel is assigned a digital value representing marking information, the apparatus comprising: a rendering circuit for defining

each pixel as either a background pixel, interior pixel, edge pixel, one line pixel, or two line pixel; and, reassigning the digital value of one or more interior pixels, edge pixels, one line pixels, or two line pixels independently.

Regarding claim 19, it is drawn to an apparatus for altering the appearance of an input digital image when printed comprising: a raster image processor for converting the image into a digital bitmap comprised of an array of pixels wherein each pixel is assigned a digital value representing marking information; a rendering circuit for defining each pixel as a background pixel, interior pixel, edge pixel, one line pixel, or two line pixel; and reassigning the digital value of one or more interior pixel, edge pixel, one line pixel, or two line pixels independently, thereby altering the appearance of the image when printed.

See above for claim 19 of US Patent 6,975,411.

The subject matter claimed in claim 19 is fully disclosed in claim 19 of the referenced US Patent 6,975,411 as follow: a raster image processor for converting the image into a digital bitmap comprised of an array of pixels wherein each pixel is assigned a digital value representing marking information; a rendering circuit for defining each pixel as a background pixel, interior pixel, edge pixel, one line pixel, or two line pixel; and reassigning the digital value of one or more interior pixel, edge pixel, one line pixel, or two line pixels independently, thereby altering the appearance of the image when printed.

Claim Objections

The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the

prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

There are two claims numbered 17. Correction is needed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsukubo et al. (Matsukubo) (Pub. No.: US 2003/0038952).

With regard to claim 1, Matsukubo discloses a method of altering the appearance of an input digital image when printed (paragraph 0012), the digital image comprised of an array of pixels and wherein each pixel is assigned a digital value representing marking information (paragraphs 0028,0122), the method comprising the steps of: defining each pixel as either a background pixel, interior pixel, edge pixel, one line pixel, or two line pixel (paragraphs 0122, 0136);

and, reassigning the digital value of one or more interior pixels, edge pixels, one line pixels, or two line pixels independently (paragraphs 0126, 0127, 0137, 0138).

With regard to claim 2, Matsukubo discloses wherein the digital image is a binary image (paragraph 0155).

With regard to claim 3, Matsukubo discloses wherein the digital image is a multi-bit image ((paragraph 0012).

With regard to claim 4, Matsukubo discloses wherein the reassigning step comprises increasing the value of edge pixels with respect to interior pixels (paragraph 0128).

With regard to claim 5, Matsukubo discloses wherein the reassigning step comprises decreasing the value of edge pixels with respect to interior pixels (paragraphs 0127, 0129).

With regard to claim 6, Matsukubo discloses further comprising performing the defining and reassigning steps two or more times (paragraphs 0126, 0127,0128).

With regard to claim 7, Matsukubo discloses a method of printing an image (paragraphs 0012) comprising the steps of: converting the image into a digital bitmap (paragraph 0027) comprised of an array of pixels wherein each pixel is assigned a digital value representing marking information (paragraphs 0028,0122); defining each pixel as a background pixel, interior pixel, edge pixel, one line pixel, or two line pixel (paragraphs 0122, 0136); and, reassigning the digital value of one or more interior pixel, edge pixel, one line pixel, or two line

pixels independently, thereby altering the appearance of the image when printed (paragraphs 0126, 0127, 0137, 0138).

With regard to claim 8, Matsukubo discloses wherein the converting step comprises converting the image to a binary digital bitmap and the reassigning step comprises reassigning the binary digital values to multi-bit digital values (paragraphs 0119,0120,0121).

With regard to claim 9, Matsukubo discloses wherein the converting step comprises converting the image to a multi-bit digital bitmap and the reassigning step comprises reassigning the binary digital values to multi-bit digital values (paragraphs 0119,0120,0121).

With regard to claim 10, Matsukubo discloses wherein the reassigning step comprises increasing the value of edge pixels with respect to interior pixels (paragraph 0128).

With regard to claim 11, Matsukubo discloses wherein the reassigning step comprises decreasing the value of edge pixels with respect to interior pixels (paragraphs 0127, 0129).

With regard to claim 12, Matsukubo discloses further comprising performing the defining and reassigning steps two or more times (paragraphs 0126, 0127,0128).

With regard to claim 13, Matsukubo discloses wherein the reassigning step further comprises reassigning the digital value of interior pixels (paragraphs 0119,0120,0121).

With regard to claim 14, Matsukubo discloses an apparatus (paragraph 0091) for altering the appearance of an input digital image when printed (paragraph 0012), the digital image comprised of an array of pixels and wherein each pixel is assigned a digital value representing marking information (paragraphs 0028), the apparatus comprising: a rendering circuit for defining each pixel as either a background pixel, interior pixel, edge pixel, one line pixel, or two line pixel (paragraphs 0122, 0136); and, reassigning the digital value of one or more interior pixels, edge pixels, one line pixels, or two line pixels independently (paragraphs 0126, 0127, 0137, 0138).

With regard to claim 15, Matsukubo discloses wherein the digital image is a binary image (paragraph 0155).

With regard to claim 16, Matsukubo discloses wherein the digital image is a multi-bit image (paragraph 0012).

With regard to claim 17, Matsukubo discloses wherein reassigning comprises increasing the value of edge pixels with respect to interior pixels (paragraph 0128).

With regard to claim 17, Matsukubo discloses wherein reassigning comprises decreasing the value of edge pixels with respect to interior pixels (paragraphs 0127, 0129).

With regard to claim 18, Matsukubo discloses wherein the rendering circuit further comprises performing defining and reassigning two or more times (paragraphs 0126, 0127,0128).

With regard to claim 19, Matsukubo discloses an apparatus (paragraph 0091) for altering the appearance of an input digital image when printed (paragraph 0012) comprising: a raster image processor for converting the image into a digital bitmap comprised of an array of pixels wherein each pixel is assigned a digital value representing marking information (paragraphs 0028); a rendering circuit for defining each pixel as a background pixel, interior pixel, edge pixel, one line pixel, or two line pixel (paragraphs 0122, 0136); and reassigning the digital value of one or more interior pixel, edge pixel, one line pixel, or two line pixels independently, thereby altering the appearance of the image when printed (paragraphs 0126, 0127, 0137, 0138).

With regard to claim 20, Matsukubo discloses wherein converting comprises converting the image to a binary digital bitmap and the reassigning step comprises reassigning the binary digital values to multi-bit digital values (paragraphs 0119,0120,0121).

With regard to claim 21, Matsukubo discloses wherein converting comprises converting the image to a multi-bit digital bitmap and the reassigning step comprises reassigning the binary digital values to multi-bit digital values (paragraphs 0119,0120,0121).

With regard to claim 22, Matsukubo discloses wherein reassigning comprises increasing the value of edge pixels with respect to interior pixels (paragraph 0128).

With regard to claim 23, Matsukubo discloses wherein reassigning step comprises decreasing the value of edge pixels with respect to interior pixels (paragraphs 0127, 0129).

With regard to claim 24, Matsukubo discloses wherein the rendering circuit performs defining and reassigning two or more times (paragraphs 0126, 0127,0128).

With regard to claim 25, Matsukubo discloses wherein reassigning further comprises reassigning the digital value of interior pixels (paragraphs 0126, 0127,0128).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang N. Vo whose telephone number is 5712701121. The examiner can normally be reached on 7:30AM-5:00PM Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Twyler M. Lamb can be reached on 5712727406. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Quang Vo

Quang N. Vo 6/21/07
Patent Examiner

TWYLER LAMB
SUPERVISORY PATENT EXAMINER